MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC10804
MC10805

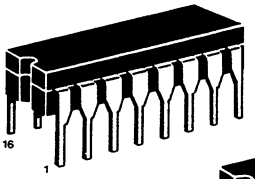
MECL — LSI
ECL/TTL INVERTING
BIDIRECTIONAL
TRANSCEIVERS WITH LATCH

BIDIRECTIONAL TRANSCEIVER WITH LATCH

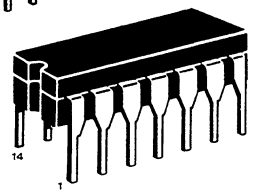
The MC10804 and MC10805 are inverting bidirectional transceivers that interface MECL logic levels with TTL logic levels. Data can be transferred directly in either direction (MECL → TTL or TTL → MECL), and an optional gated latch is also provided. Logic levels are inverted during transfers. The MC10804 is a 4-bit version in the 16-pin package, and the MC10805 is a 5-bit version in the 20-pin package.

The MC10804 and MC10805 are members of the high performance M10800 MECL/LSI processor family. They make it possible to easily interface to MOS memories, TTL compatible peripherals, or existing TTL subsystems.

- Bidirectional Translation
- Power Supplies: +5.0 Volts and -5.2 Volts
- TTL Three-State Outputs
  - Sink 50 mA
  - Source 5.0 mA
- Standard MECL 50 Ohm Drive Outputs
- Latch — Can Be Bypassed for High Speed

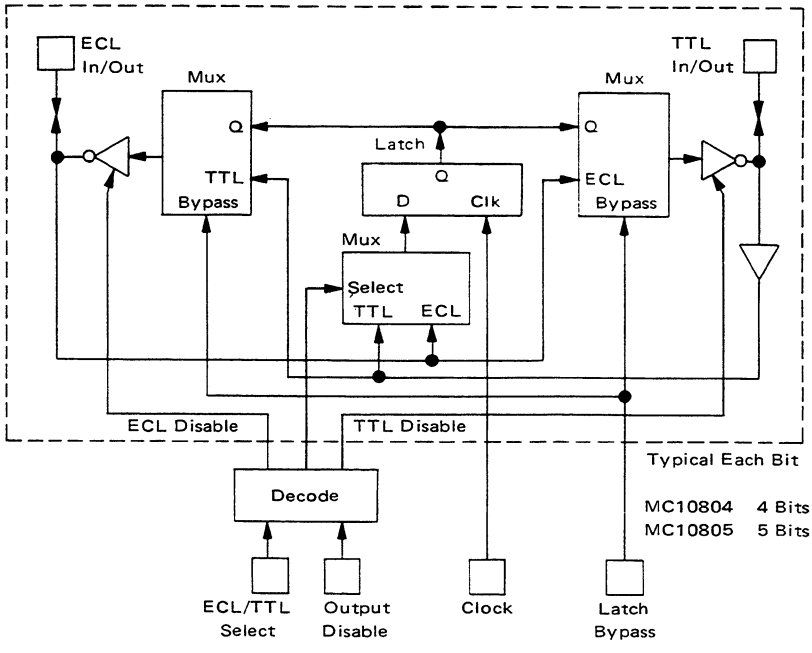


L SUFFIX
CERAMIC PACKAGE
CASE 620-02
MC10804

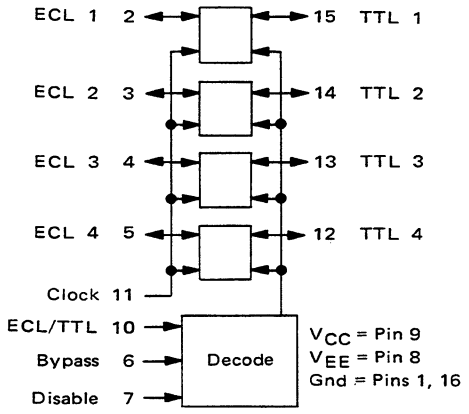


L SUFFIX
CERAMIC PACKAGE
CASE 732-03
MC10805

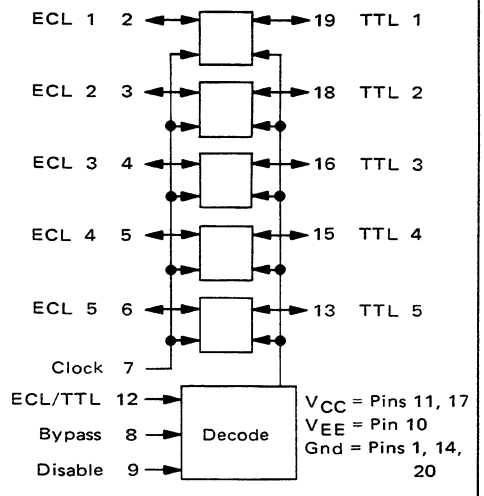
BLOCK DIAGRAM



MC10804



MC10805



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DS 9652
(Replacing ADI-500)

FUNCTIONAL DESCRIPTION

The MC10804 consists of a function decode section, a clock buffer, and four identical bit channels which perform the ECL-TTL translation. Each bit consists of a bidirectional ECL port, a bidirectional TTL port, and a latch. The MC10805 contains the same circuit blocks, but has five instead of four bits translation.

Three logic pins control the function selection. These pins, along with the clock, all operate at standard MECL levels. The block diagram and truth table define the functions. The individual pin descriptions are as follows:

Output Disable

The Output Disable, when at V_{IL}, disables both the ECL and TTL output buffers. That is, both are forced to high-impedance states. When the Output Disable is at V_{IH} the ECL/TTL translation takes place normally, and the appropriate output ports enabled by the ECL/TTL select are active. Regardless of the state of the Output Disable pin, clocked data can be loaded into the latch from the selected input port.

ECL/TTL Select

The ECL/TTL Select pin controls the direction of data transfers. When at V_{IL}, the TTL-to-ECL direction is selected. In this case, the TTL output drivers are disabled, data is input to the latch from the TTL port, and data is output onto the ECL port. When the select pin is at V_{IH}, the ECL-to-TTL direction is selected and the function is the reverse of that just described.

Latch Bypass

The Latch Bypass select line bypasses the latch circuitry for the fast data transfer. When the select line is at V_{IL}, the data is directed to both the latch input and the output buffer simultaneously. This feature enhances the speed of translation because the delay through the latch is bypassed. When the Latch Bypass pin is at V_{IH}, the data must first go into the latch then be sent to the output ports.

Clock

The Clock input is common to all latches and controls the storage of data. When the Clock is at V_{IL} the latch is open and data ripples through from the D input to the Q output. Data is stored or latched on the V_{IL}-to-V_{IH} transition of the Clock input.

NEGATIVE LOGIC DIAGRAM

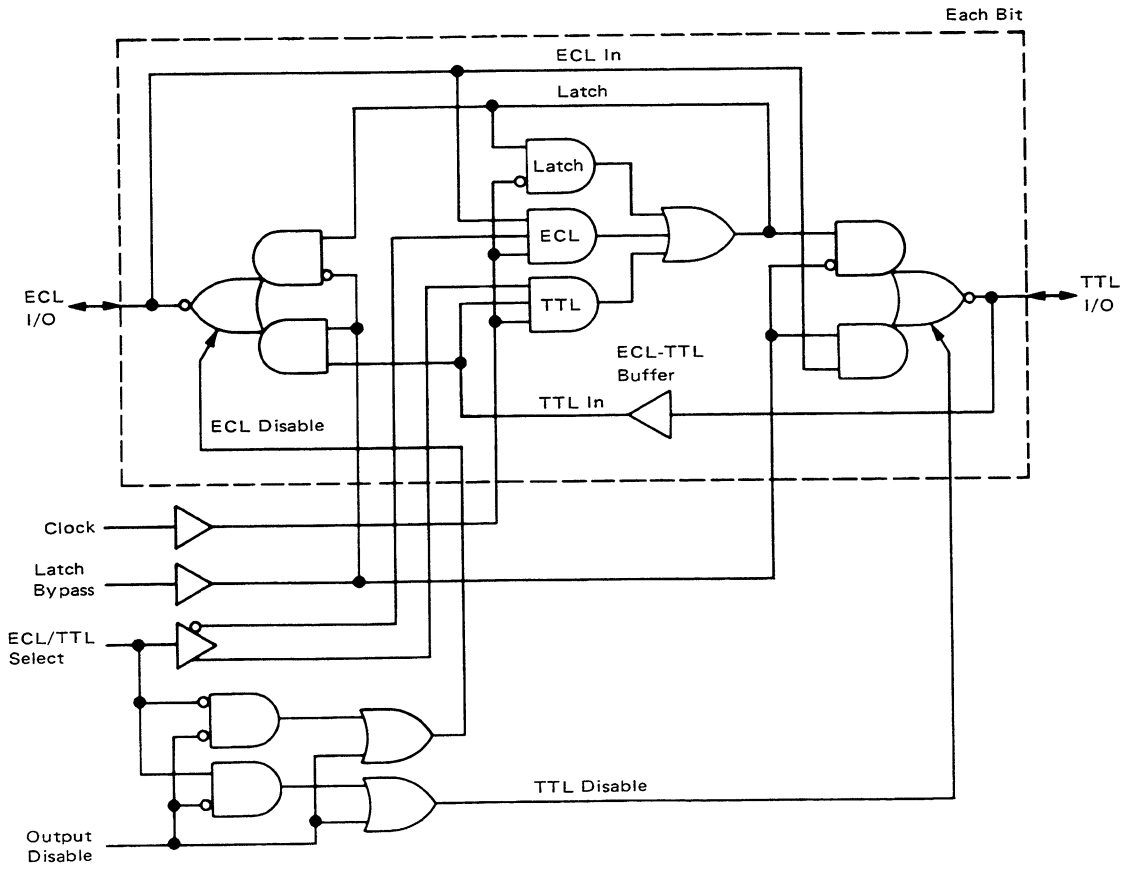
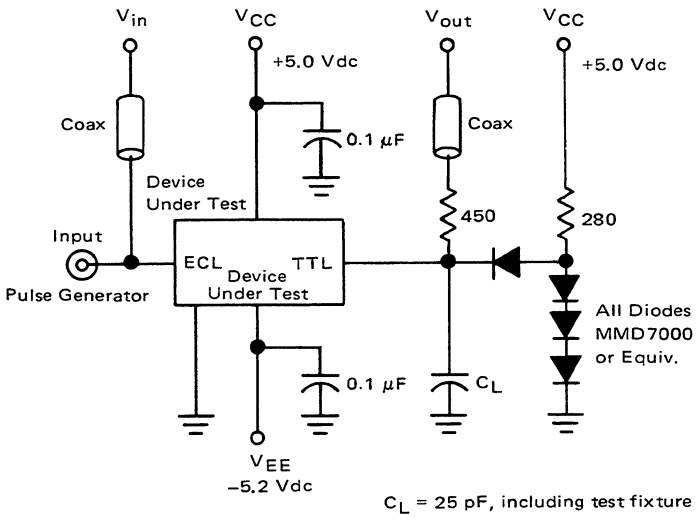
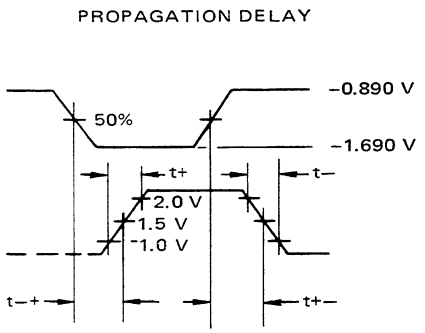


FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C
FOR PROPAGATION DELAY FROM MECL INPUT
TO TTL OUTPUT WITH TTL LOAD



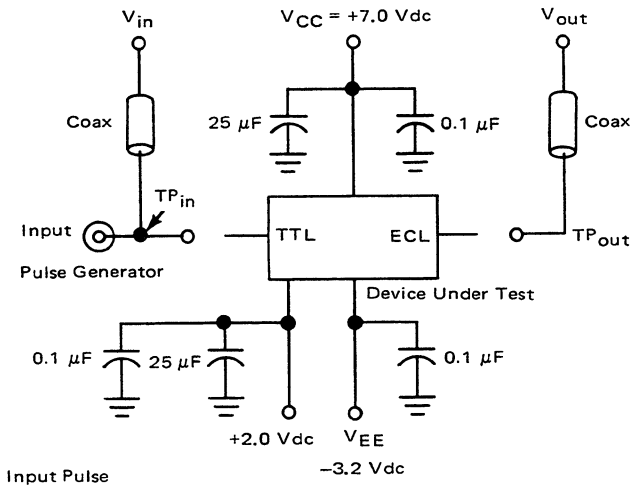


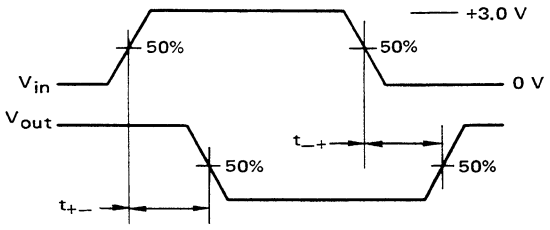
C_L = 25 pF, including test fixture

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C
FOR PROPAGATION DELAY FROM TTL INPUT
TO ECL OUTPUT



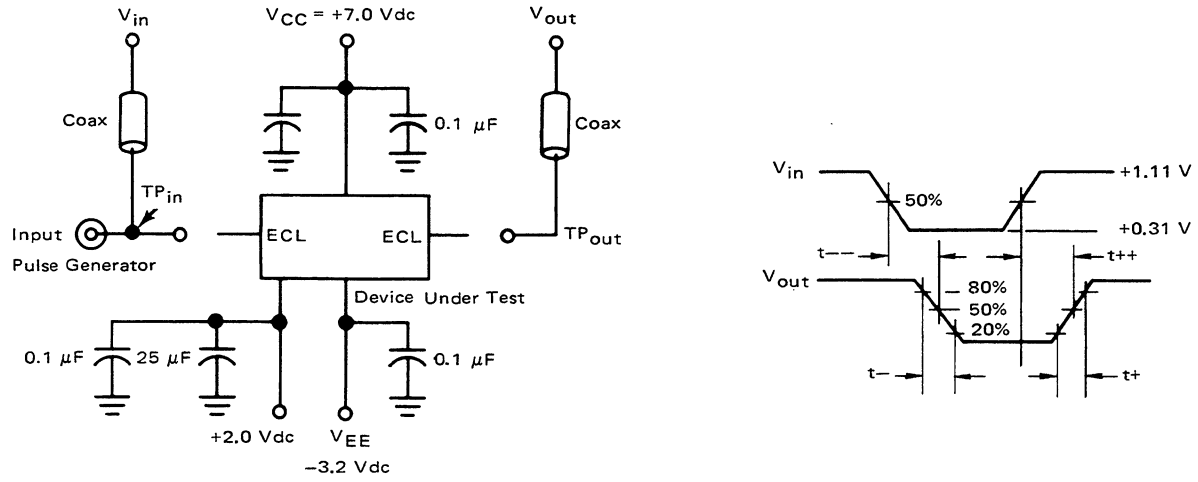


Input Pulse
t+ = t− = 5.5 ± 0.5 ns
(10% - 90%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

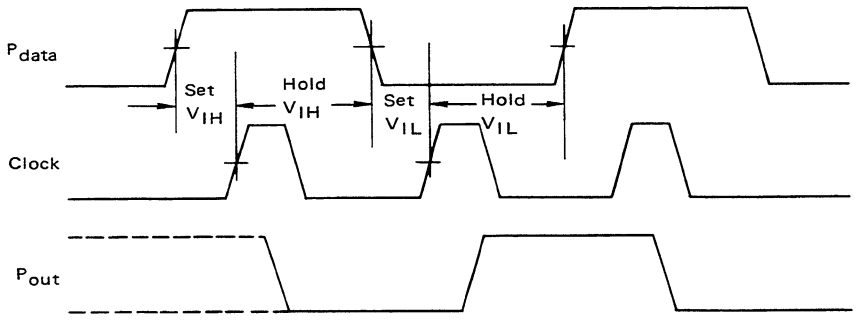
FIGURE 3 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C
FOR PROPAGATION DELAY FROM ECL SELECT
INPUT TO ECL OUTPUT



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

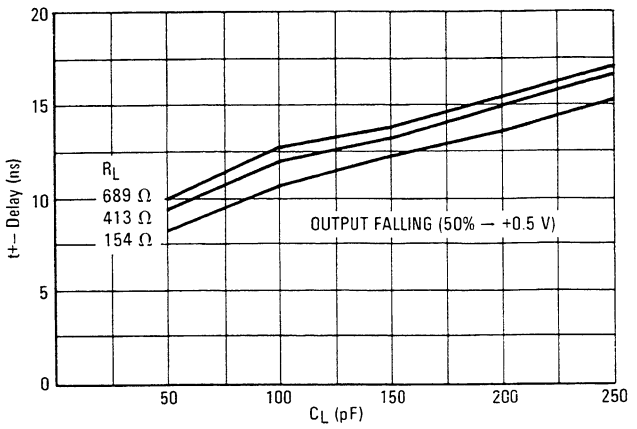
FIGURE 4 — SETUP AND HOLD TIME WAVEFORMS



* For These Tests, $P_{out} = \overline{P_{data}}$ in All Cases.

FIGURE 5 — MC10805 ECL – TTL DELAY (Latch Bypassed) versus CAPACITIVE LOAD
(T_A = +25°C, V_{CC} = 5.0 V)

A. OUTPUT FALLING (50% – THRESHOLD)



B. OUTPUT RISING (50% – THRESHOLD)

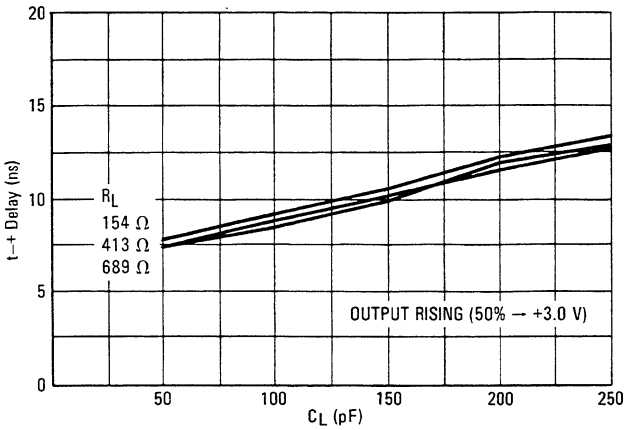
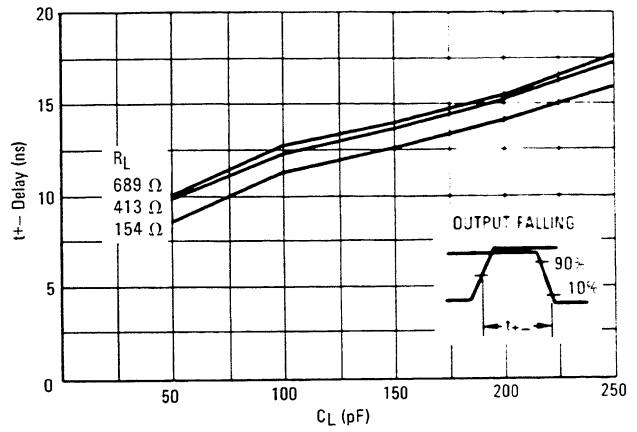
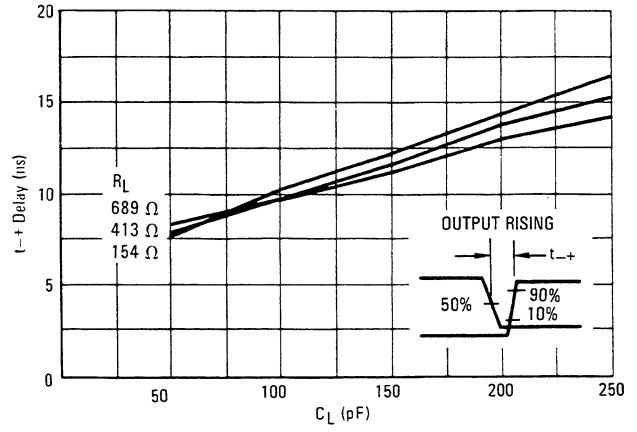


FIGURE 6 — MC10805 ECL – TTL DELAY (Latch Bypassed) versus CAPACITIVE LOAD
(T_A = +25°C, V_{CC} = 5.0 V)

A. OUTPUT FALLING (50% – 10%)



B. OUTPUT RISING (50% – 90%)



MC10805 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+4.75 to +5.25 -4.94 to -5.46	Vdc Vdc
Operating Temperature (Functional)	T_A	0 to +75	°C
Max Output Drive — ECL — TTL	— —	50 Ω to -2.0 Vdc V_{CC} = 0.6 V @ 50 mA	— —
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)							
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}
0°C	-0.845	-1.870	-1.130	-1.485	+2.0	+0.8	+5.00	-5.20
+25°C	-0.810	-1.850	-1.105	-1.475	+2.0	+0.8	+5.00	-5.20
+75°C	-0.720	-1.830	-1.045	-1.445	+2.0	+0.7	+5.00	-5.20

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC10805 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_{EE}	10	—	—	—	-145	—	—	mAdc	—	—	—	—	—	—	11, 17	10	1, 14 20	—
Positive Power Supply Drain Current	I_{CCH}	11, 17	—	—	—	+100	—	—	mAdc	9, 12	2, 3, 4, 5, 6, 8	—	—	—	—	↓	↓	↓	*
	I_{CCL}	11, 17	—	—	—	+70	—	—	mAdc	—	9	—			—				—
Input Current	I_{inH}	19	—	—	—	45	—	—	μAdc	19	—	—	—	—	—				—
		8	—	—	—	350	—	—	μAdc	8	—	—	—	—	—				—
		2	—	—	—	485	—	—	μAdc	2	—	—	—	—	—				—
	I_{inL}	8	—	—	0.5	—	—	—	μAdc	—	8	—	—	—	—				—
ECL High Output Voltage	V_{OH}	2	-1.005	-0.845	-0.960	-0.810	-0.900	-0.720	Vdc	7, 9	8, 12	—	—	—	19				—
ECL Low Output Voltage	V_{OL}	2	-1.950	-1.660	-1.950	-1.650	-1.950	-1.620	Vdc	7, 9	8, 12	—	—	19	—				—
ECL High Threshold Voltage***	V_{OHA}	2	-1.025	—	-0.980	—	-0.920	—	Vdc	7, 9	8	—	12	—	19				—
ECL Low Threshold Voltage	V_{OLA}	2	—	-1.640	—	-1.630	—	-1.600	Vdc	7, 9**	12	8	—	—	19				—
ECL Cutoff Voltage	V_{OLZ}	2	—	-1.960	—	-1.960	—	-1.960	Vdc	—	9	—	—	—	—				—
TTL High Output Voltage	V_{OHT}	19	+2.400	—	+2.400	—	+2.400	—	Vdc	7, 9, 12	2, 8	—	—	—	—				-24 mA
TTL Low Output Voltage	V_{OLT1}	19	—	+0.500	—	+0.500	—	+0.500	Vdc	2, 7, 9, 12	8	—	—	—	—				25 mA
	V_{OLT2}	19	—	+0.600	—	+0.600	—	+0.600	Vdc	2, 7, 9, 12	8	—	—	—	—				50 mA
TTL High Threshold Voltage***	V_{OHAT}	19	+2.500	—	+2.500	—	+2.500	—	Vdc	9, 12	7, 8	—	2	—	—				-24 mA
TTL Low Threshold Voltage	V_{OLAT1}	19	—	+0.500	—	+0.500	—	+0.500	Vdc	9, 12	7, 8	2	—	—	—				25 mA
	V_{OLAT2}	19	—	+0.600	—	+0.600	—	+0.600	Vdc	9, 12	7, 8	2	—	—	—				50 mA
TTL Cutoff Leakage Current	I_{OHZ}	19	—	+100	—	+100	—	+100	μAdc	2	8, 9	—	—	19	—				—
	I_{OLZ}	19	—	-50	—	-50	—	-50	μAdc	2	8, 9	—	—	—	19			↓	—
TTL Short Circuit Current	I_{SC}	19	—	—	—	170	—	—	mAdc	7, 9, 12	2, 8	—	—	—	—	↓	↓	1, 14, 19, 20	—

*-5.0 mA sourced at output Pins 13, 15, 16, 18, 19

**Requires the following preset: V_{IH} at Pin 9; V_{IL} at Pins 8, 12; V_{IHT} at Pin 19; then clock once (⊔)

***TTL threshold inputs are the same as V_{IHT} and V_{ILT}

MC10804 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+4.75 to +5.25 -4.94 to -5.46	Vdc Vdc
Operating Temperature (Functional)	T_A	0 to +75	°C
Max Output Drive — ECL — TTL	— —	50 Ω to -2.0 Vdc V_{CC} = 0.6 V @ 50 mA	— —
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts)							
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}
0°C	-0.845	-1.870	-1.130	-1.485	+2.0	+0.8	+5.00	-5.20
+25°C	-0.810	-1.850	-1.105	-1.475	+2.0	+0.8	+5.00	-5.20
+75°C	-0.720	-1.830	-1.045	-1.445	+2.0	+0.7	+5.00	-5.20

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC10804 TEST LIMITS 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_{EE}	8	—	-125	—	-125	—	-125	mAdc	—	—	—	—	—	—	9	8	1, 16	—
Positive Power Supply Drain Current	I_{CCH}	9	—	+60	—	+60	—	+60	mAdc	7, 10	2, 3, 4, 5, 6	—	—	—	—				*
	I_{CCL}	9	—	+45	—	+45	—	+45	mAdc	—	7	—	—	—	—				—
Input Current	I_{inH}	15	—	—	—	45	—	—	μAdc	15	—	—	—	—	—				—
		6	—	—	—	350	—	—	μAdc	6	—	—	—	—	—				—
		2	—	—	—	485	—	—	μAdc	2	—	—	—	—	—				—
	I_{inL}	6	—	—	0.5	—	—	—	μAdc	—	6	—	—	—	—				—
ECL High Output Voltage	V_{OH}	2	-1.005	-0.845	-0.960	-0.810	-0.900	-0.720	Vdc	7, 11	6, 10	—	—	—	15				—
ECL Low Output Voltage	V_{OL}	2	-1.950	-1.660	-1.950	-1.650	-1.950	-1.620	Vdc	7, 11	6, 10	—	—	15	—				—
ECL High Threshold Voltage***	V_{OHA}	2	-1.025	—	-0.980	—	-0.920	—	Vdc	7, 11	6	—	10	—	15				—
ECL Low Threshold Voltage	V_{OLA}	2	—	-1.640	—	-1.630	—	-1.600	Vdc	7, 11**	10	6	—	—	15				—
ECL Cutoff Voltage	V_{OLZ}	2	—	-1.960	—	-1.960	—	-1.960	Vdc	—	7	—	—	—	—				—
TTL High Output Voltage	V_{OHT}	15	+2.400	—	+2.400	—	+2.400	—	Vdc	7, 10, 11	2, 6	—	—	—	—				-24 mA
TTL Low Output Voltage	V_{OLT1}	15	—	+0.500	—	+0.500	—	+0.500	Vdc	2, 7, 10, 11	6	—	—	—	—				25 mA
	V_{OLT2}	15	—	+0.600	—	+0.600	—	+0.600	Vdc	2, 7, 10, 11	6	—	—	—	—				50 mA
TTL High Threshold Voltage***	V_{OHAT}	15	+2.500	—	+2.500	—	+2.500	—	Vdc	7, 10	6, 11	—	2	—	—				-24 mA
TTL Low Threshold Voltage	V_{OLAT1}	15	—	+0.500	—	+0.500	—	+0.500	Vdc	7, 10	6, 11	2	—	—	—				25 mA
	V_{OLAT2}	15	—	+0.600	—	+0.600	—	+0.600	Vdc	7, 10	6, 11	2	—	—	—				50 mA
TTL Cutoff Leakage Current	I_{OHZ}	15	—	+100	—	+100	—	+100	μAdc	2	6, 7	—	—	15	—				—
	I_{OLZ}	15	—	-50	—	50	—	-50	μAdc	2	6, 7	—	—	—	15				—
TTL Short Circuit Current	I_{SC}	15	—	—	—	170	—	—	mAdc	7, 10, 11	2, 6	—	—	—	—			1, 15, 16	—

*-5.0 mA sourced at output Pins 12, 13, 14, 15

**Requires the following preset: V_{IH} at Pin 7; V_{IL} at Pins 6, 10; V_{IHT} at Pin 15; then clock once (⊔)

***TTL threshold inputs are the same as V_{IHT} and V_{ILT}

MC10805 SETUP AND HOLD TIMES (NANOSECONDS AT 25°C)

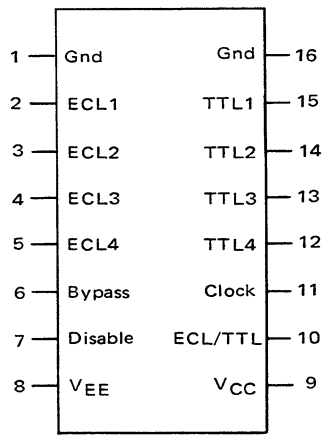
	Setup (Min)	Hold (Min)
1. ECL 1-5 to Clock	3.0	5.0
2. TTL 1-5 to Clock	4.0	4.0
3. ECL/TTL Select to Clock	6.0	3.0

MC10805 PROPAGATION DELAYS (NANOSECONDS AT 25°C)

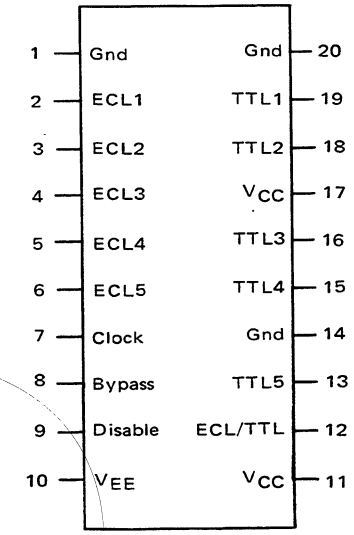
	Mode	Load	Max
1. ECL 1-5 → TTL 1-5	Latch Bypassed	TTL	8.5
2. TTL 1-5 → ECL 1-5	Latch Bypassed		8.5
3. ECL 1-5 → TTL 1-5	Via Latch	TTL	12
4. TTL 1-5 → ECL 1-5	Via Latch		14
5. Latch Bypass → TTL 1-5		TTL	14
6. Latch Bypass → ECL 1-5			10.5
7. Output Disable → TTL 1-5		TTL	24
8. Output Disable → ECL 1-5			11.5
9. ECL/TTL Select → TTL 1-5		TTL	24
10. ECL/TTL Select → ECL 1-5			11
11. Clock → TTL 1-5		TTL	14
12. Clock → ECL 1-5			14

PIN ASSIGNMENTS

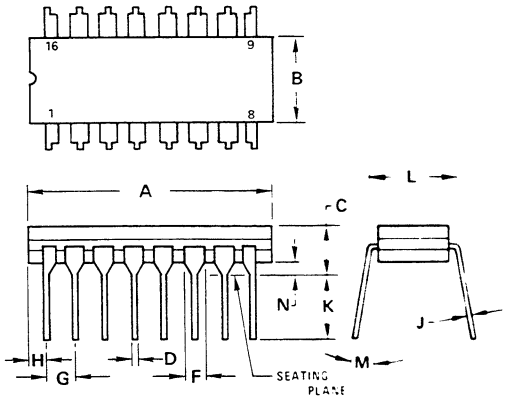
MC10804



MC10805



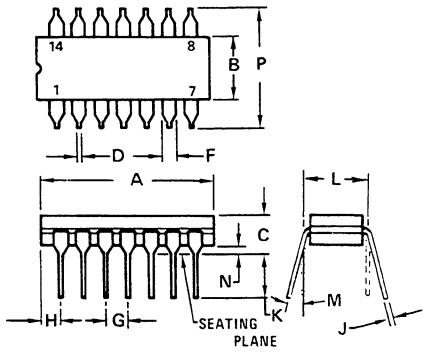
PACKAGE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 620-02



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH MO-001 AA OUTLINE SHALL APPLY.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. LEADS WITHIN 0.25mm (0.010) DIA OF TRUE POSITION AT SEATING PLANE AND MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.45	1.60	0.057	0.063
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030

CASE 732-03

TRUTH TABLE

SELECT INPUTS (ECL LEVELS, H = -0.9 V, L = -1.7 V)				FUNCTION		
Output Disable	TTL/ECL Select	Latch Bypass	Clock (2)	Latch (1)	TTL I/O (H = 2.4 V, L = 0.5 V)	ECL I/O (H = -0.9 V, L = -1.7 V)
H	H	H	H	* Q = H * Q = L	Output = $\overline{Q}$ = L = H	Off Off
H	H	H	L	Q = ECL Input = H L	Output = $\overline{Q}$ = L = H	Input = H = L
H	H	L	H	* *	Output = $\overline{ECL}$ = L = H	Input = H = L
H	H	L	L	Q = ECL Input = H = L	Output = $\overline{ECL}$ = L = H	Input = H = L
H	L	H	H	* Q = H * Q = L	Off Off	Output = $\overline{Q}$ = L = H
H	L	H	L	Q = TTL Input = H = L	Input = H = L	Output = $\overline{Q}$ = L = H
H	L	L	H	* *	Input = H = L	Output = $\overline{TTL}$ = L = H
H	L	L	L	Q = TTL Input = H = L	Input = H = L	Output = $\overline{TTL}$ = L = H
L	H	H	H	*	Off	Off
L	H	H	L	Q = ECL Input = H = L	Off Off	Input = H = L
L	H	L	H	*	Off	Off
L	H	L	L	Q = ECL Input = H = L	Off Off	Input = H = L
L	L	H	H	*	Off	Off
L	L	H	L	Q = TTL Input = H = L	Input = H = L	Off
L	L	L	H	*	Off	Off
L	L	L	L	Q = TTL Input = H = L	Input = H = L	Off

NOTES: (1) * Denotes "NO CHANGE" (2) Latch transfers data when clock is "L" and stores data when clock is "H".

MC10804 SETUP AND HOLD TIMES (NANOSECONDS AT 25°C)

	Setup (Min)	Hold (Min)
1. ECL 1-4 to Clock	3.0	5.0
2. TTL 1-4 to Clock	4.0	4.0
3. ECL/TTL Select to Clock	6.0	3.0

MC10804 PROPAGATION DELAY TIMES (NANOSECONDS AT 25°C)

	Mode	Load	Max
1. ECL 1-4 → TTL 1-4	Latch Bypassed	TTL	8.5
2. TTL 1-4 → ECL 1-4	Latch Bypassed		8.5
3. ECL 1-4 → TTL 1-4	Via Latch	TTL	12
4. TTL 1-4 → ECL 1-4	Via Latch		14
5. Latch Bypass → TTL 1-4 6. Latch Bypass → ECL 1-4		TTL	14 10.5
7. Output Disable → TTL 1-4 8. Output Disable → ECL 1-4		TTL	24 11.5
9. ECL/TTL Select → TTL 1-4 10. ECL/TTL Select → ECL 1-4		TTL	24 11
11. Clock → TTL 1-4 12. Clock → ECL 1-4		TTL	14 14

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